Planar Channel-All-Around (P-CAA) Oxide FETs with One-step Process for High-density 1T1C 3D DRAM

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DRAM technology is getting more and more important with the rapidly increasing computational requirements from artificial intelligence (AI). To increase the memory density, bit cell size needs to be further shirked. Conventional planar DRAM technology is suffering from the device miniaturization with existing structure when it approaches physical limits below 10nm. 3D DRAM technology provides an alternative way to increase memory density other than scaling-down by allowing memory arrays to be fabricated vertically. Therefore, some silicon-based 3D DRAM architectures been proposed and demonstrated [1,2]. However, these approaches have the challenges like high-quality epitaxial growth of Si/SiGe. Recently, the oxide semiconductor is getting tremendous attentions in the DRAM field due to the relatively high mobility and extremely low leakage current. Furthermore, the oxide semiconductor transistor can be fabricated by low-temperature atomic layer deposition process, making it a promising candidate for 3D DRAM technology.

We have proposed a novel planar channel-all-around (P-CAA) IGZO FET for 3D DRAM application and the schematic diagram is shown in Fig. 1 (a). The bit cell of the design consists of a channel-all-around oxide transistor and a capacitor (1T1C). The vertically located word-line design makes it suitable for monolithic stacking. Besides, the novel one-step process dramatically increases the fabrication efficiency due to the shared critical process steps like lithography and etching. Fig.1 (b) shows the cross-sectional TEM image of the fabricated 4-layer stacked bit cells which demonstrate the detailed construction.

The transfer characteristics of the IGZO FETs on top and bottom layers in Fig. 2(a) show good performance uniformity of the devices on different layers. After 10^{10} duty cycle test as is shown in Fig.2 (b), there's no obvious performance degradation, proving the robustness of P-CAA IGZO FETs.

References

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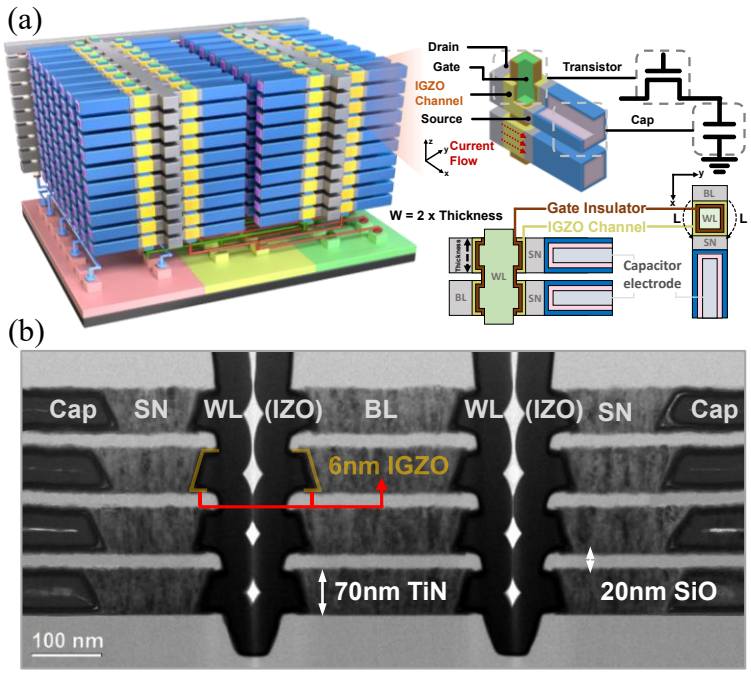

Fig.1 (a) The schematic of the P-CAA oxide FETs for high-density 3D DRAM. (b) Cross-sectional TEM image of the fabricated P-CAA FETs.

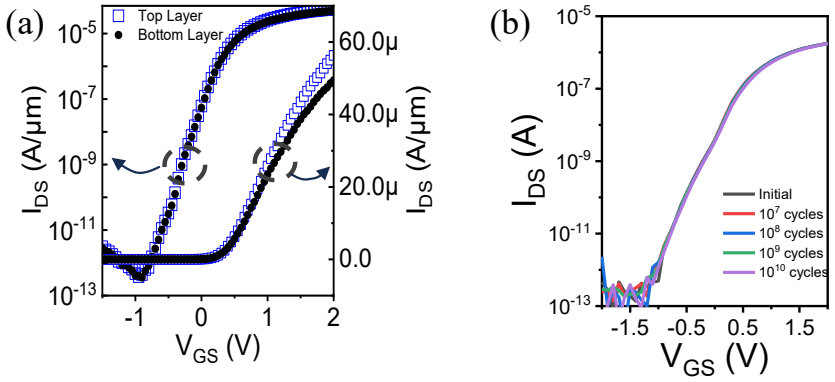

Fig.2 (a) Transfer curves of the fabricated P-CAA IGZO FETs on different layers. (b) Transfer characteristics of the transistor after 10^{10} endurance test.